Analysis of Interconnection Delay on Very High-Speed LSI/VLSI Chips Using an MIS Microstrip Line Model

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Abstract—**Using an MIS (metal–insulator–semiconductor) microstrip-line model for interconnection and its equivalent circuit representation, on-chip interconnection delay in very high-speed LSI/VLSI's is analyzed in the time domain, changing interconnection geometry, substrate resistivity, and terminal conditions. The results show the following: 1) the "lumped capacitance" approximation is inapplicable for interconnections in very high-speed LSI/VLSI's (t_{pd} of below 100–200 ps); 2) as compared to the semi-insulating substrate, the presence of the slow-wave mode and mode transition in the semiconducting substrates causes 1.5–2 times increase in the delay time and 2–10 times increase in the rise time; and 3) in order to realize propagation delay times of less than 100 ps per gate at LSI/VLSI levels, the effective signal source resistance of the gate should be less than 500 Ω so as to long interconnections.**

I. Introduction

DEVELOPMENT of very high-speed integrated circuits is currently of great technological interest, owing to an ever increasing demand for higher speeds in the areas of high-speed computation, signal processing, data links, and related instrumentation. Indeed, LSI/VLSI's with an average propagation delay per gate t_{pd} of 100 ps or below will have a great technological impact on these areas, judging from the speed performance of currently available integrated circuits. In the small- to medium-scale integration levels, propagation delay times in the 10–30-ps range have already been realized with GaAs MESFET, HEMT, Josephson Junction, and Si NMOS technologies. If such speeds are to be realized in LSI/VLSI integration levels, however, on-chip interconnection delay and crosstalk are expected to become important problems due to the increased length of interconnections. Proper design considerations to minimize them should be paid in order to take full advantage of the inherent speed capability of the device.

The purpose of the present paper is to investigate the on-chip interconnection delay in very high-speed integrated circuits, using an MIS (metal–insulator–semiconductor) microstrip line model. Effects of interconnection geometry, substrate conductivity, and device driving capability on propagation delay, distortion, and multiple reflection are analyzed. The problem of crosstalk due to interconnection is analyzed in a separate paper [1], using a coupled multiconductor MIS stripline model.

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The result of this paper shows that the conventional "lumped capacitance" approximation for interconnections is no longer adequate for the design of LSI/VLSI's with t_{pd} of below 100 ps; therefore, the interconnections should be treated as miniaturized microwave networks. In the semiconducting substrate, wave propagation is dispersive due to slow-wave mode propagation and mode transition. Owing to this, propagation delay and rise times of high-speed pulses are deteriorated in the semiconducting substrate as compared with the semi-insulating substrate. It is also shown that the driving capability of the device to drive long interconnections is essentially important for realization of very high-speed LSI/VLSI's.

II. Model and Method of Analysis

A. Length of Interconnections in LSI/VLSI's

The average interconnection length L per gate on LSI/VLSI chips is known to increase with the gate count G, as in the following empirical formula:

$$L = KG^{\alpha}\sqrt{A} \tag{1}$$

where K and α are empirical constants, and A is the logic cell layout area. Equation (1) can also be derived theoretically [2], [3] on the basis of the Rent's rule [4] concerning the pin versus gate count relationship. Using the reported values of K and α [3], [5], [6], the average interconnection length is plotted versus gate count in Fig. 1. As seen in Fig. 1, the average interconnection length becomes 0.5–5 mm for $G = 10^3$–10^4. Thus, speed is limited not only by the device speed itself, but by the fact that each gate should drive interconnections at a high speed. Previously, this effect has been treated in terms of the "lumped capacitance" of interconnections [6]–[10]. However, since the propagation time of an ideal TEM wave over 1-mm distance is typically 8–10 ps on a semiconductor substrate ($\epsilon_r = 12$–13), validity of such an approach becomes very doubtful in high-speed LSI/VLSI's. Thus, the transmission-line effects of interconnections have to be investigated.

B. An MIS Microstrip Line Model and Approach for Analysis

An MIS-type single microstrip line model shown in Fig. 2 is used for the analysis. It is a microstrip line formed on a surface passivated semiconductor substrate with a metal-

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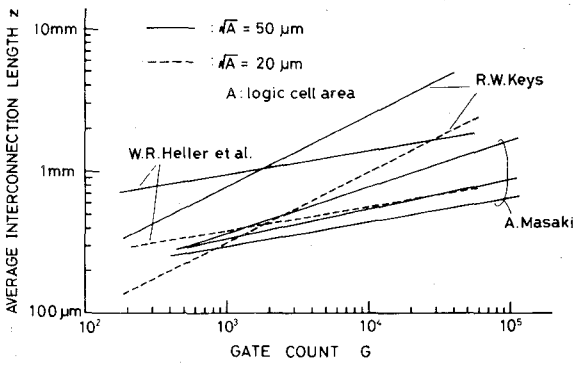

Fig. 1. The average interconnection length plotted versus gate count G. A is the logic cell area.

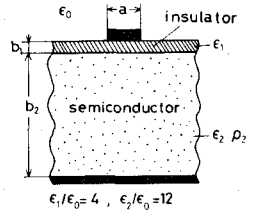

Fig. 2. An MIS (metal–insulator–semiconductor) microstrip line model for interconnection.

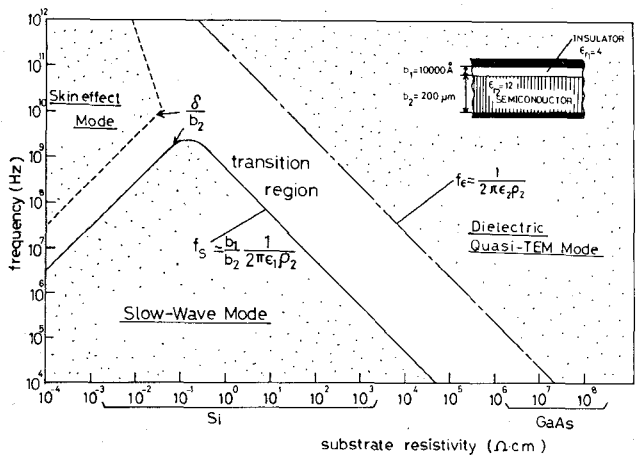

Fig. 3. Resistivity-frequency mode chart of the MIS microstrip line. is the skin depth in semiconductor, and ρ is the semiconductor resistivity.

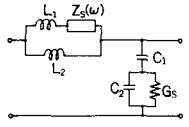

Fig. 4. Equivalent circuit per unit length of the MIS microstrip line.

lized back. In practice, a metallized back is not necessarily formed. However, when the chip is mounted, an equivalent situation is usually brought about.

Owing to the finite conductivity of the semiconductor substrate, a rigorous analysis of wave propagation along such a stripline is difficult, and can be done only numerically in the frequency domain, using the spectral-domain method [11], [12], mode-matching method [12], or by the finite-element method [13]. But these complicated numerical procedures require large computational resources and are generally time consuming. Additionally, they tend to run into difficulties of divergence from the true solution if the initialization is inappropriate [13]. Thus, they do not seem to be practical for a quick estimate of on-chip delay in the time domain, changing the parameters over wide ranges.

The equivalent circuit approach by Hasegawa *et al.* [14]–[16], which allows a closed-form analysis in the frequency domains, is employed here as the basis for the time-domain analysis. In this approach, the fundamental TM mode of an MIS parallel plate waveguide is rigorously analyzed [13], [17], and an equivalent circuit representation for an MIS microstrip line is set up on the basis of physical understanding of the modes. Then, each equivalent circuit parameter is evaluated to take account of the fringing effect of the microstrip of the finite width.

C. Propagation Modes

The resistivity-frequency mode chart of the MIS microstrip line based on such an analysis is schemetically shown in Fig. 3. When the substrate conductivity is low, the substrate acts like an insulator, and the dielectric quasi-TEM mode propagates. When the substrate conductivity is high, the substrate acts like a imperfect metal wall with a large skin effect, resulting in a skin-effect mode. A remarkable point concerning the MIS waveguide is that the slow-wave mode propagates when the substrate is semiconducting and the frequency is low. In the low-frequency limit, electric-field lines do not penetrate into the semiconductor, whereas the magnetic-field lines can fully penetrate into it. This results in spatially separated storage of electric and magnetic energies, leading to propagation of the slow-wave mode. It should be noted that the slow-wave mode region extends into the gigahertz range at a certain resistivity. Propagation of such a mode was experimentally confirmed by Hasegawa *et al.* [13], [18], and several authors have investigated its application to variable delay lines [19]–[21]. Its application to wavelength reduction in GaAs MMIC's using an MIS coplanar stripline was proposed [22] and analyzed [12]. It will be shown here that the slow-wave mode and the related mode transition have large effects on the fast-pulse transmission on semiconductor chips.

D. Equivalent Circuit Representation

The equivalent circuit representation per unit length of the MIS microstrip line used in this study is shown in Fig. 4. The representation is slightly modified from the original one in [13] to take account of the mode transition more appropriately. In Fig. 4, C_1 is the insulator capacitance, C_2 and G_s are the capacitance and transverse conductance of the semiconductor. L_1 is the inductance of the insulator, L_2 is the inductance of the air region, and $Z_s(\omega)$ is the impedance of the semiconductor region, including the semiconductor inductance and longitudinal resistance. Due to the skin effect in the semiconductor, the semiconductor impedance is frequency dependent. The derivation of the explicit formulas for the circuit elements in the equivalent circuits is summarized in the Appendix. In particular, an

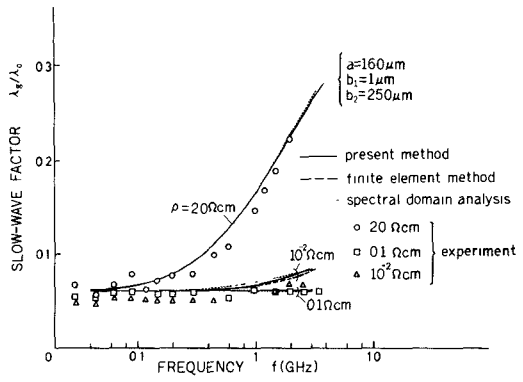

Fig. 5. Plots of the slow-wave factor as obtained by the present and other theories [11], [13] together with experimental data [14]. In the case of $\rho = 0.1\ \Omega\cdot$cm and $\rho = 20\ \Omega\cdot$cm, the agreement between the present results and those by the finite-element method is extremely good; therefore, one curve representing two sets of results was drawn in the figure.

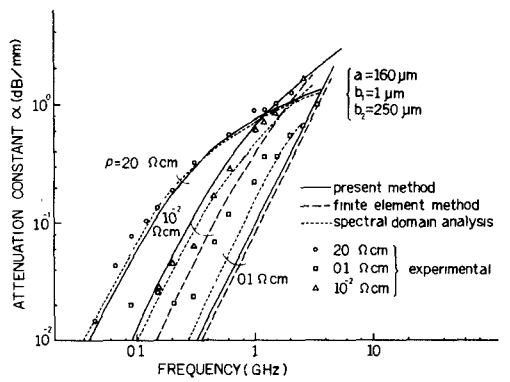

Fig. 6. Plots of the attenuation constant as obtained by the present and other theories [11], [13] together with experimental data [14]. Present results are again in good agreement with the finite-element method in the case of $\rho = 20\ \Omega\cdot$cm, where two curves merged together.

analytic expression for $Z_s(\omega)$ is newly derived in order to improve the accuracy in treating the skin-effect loss under the finite width microstrip more accurately than our previous analyses [14]–[16] and the analysis by Hughes and White [17].

E. Results of Frequency-Domain Analysis

In order to check the validity of the present approach, transfer characteristics in the frequency domain, calculated using the equivalent circuit shown in Fig. 4, are compared with the results of the numerical analyses [11], [13] and with our previous experimental data [14]. Plots of the slow-wave factor and the attenuation constant are shown in Figs. 5 and 6, respectively. Agreement is very good, particularly for the practically important resistivity range of above $10^{-1}\ \Omega\cdot$cm. The experimentally observed attenuation constant is found to be somewhat higher than theoretical values, and this is presumably due to the metallic loss which is not considered in the present theory. The good agreement obtained here seems to indicate that the present method may be useful not only to pulse transmission calculation but also to analysis and design of MIS transmission lines for microwave analog applications.

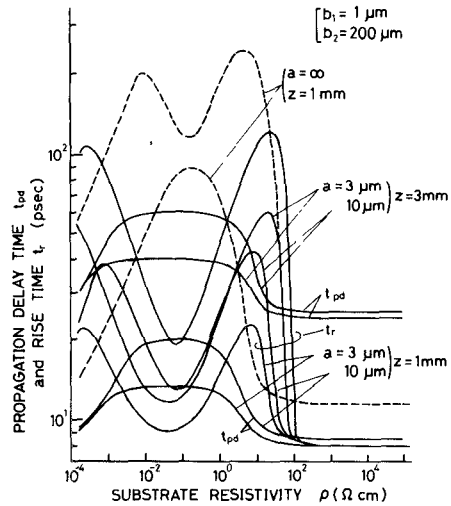

Fig. 7. Calculated propagation delay time and rise time of the step response for a semi-infinite interconnection (or matched termination). The rise time of the input pulse is assumed to be 8 ps.

III. Time-Domain Results and Discussion

A. Procedure for Transient Calculation

Calculation of the transient waveforms were done in the following way. Given an interconnection geometry, the equivalent circuit parameters were computed. By substituting these values into the analytic expressions for the characteristic impedance and propagation constants based on the equivalent circuit in Fig. 4, transient waveforms under arbitrary excitation and termination conditions can be calculated by the inverse Laplace transform. The inverse Laplace transform was carried out numerically using the standard trigonometric function expansion method.

B. Matched Termination

Fig. 7 shows the calculated delay time (time to 50-percent rise) and rise time (time between 10–90-percent rise) of the step response as a function of the semiconductor substrate resistivity. The response is calculated at positions with distance of $z = 1$ and 3 mm from the signal source. The interconnection length is assumed to be semi-infinite or the line is assumed to be terminated with a hypothetical matched load. The behavior of the delay and rise times versus substrate resistivity can be explained in terms of the three fundamental modes, i.e., the dielectric quasi-TEM mode, slow-wave mode, and skin-effect mode. An increase of the delay time at the mid-resistivity range is due to the slow-wave mode, and rise-time peaks on both sides of the delay time-peak are due to the mode transition from the slow-mode either to the dielectric quasi-TEM mode or to the skin-effect mode. It should be noted that considerable deterioration of the pulse response takes place at resistivities of 1–100 $\Omega\cdot$cm, which are frequently used in Si technology. The basic reason for this deterioration of rise time associated with the transition from the slow-wave mode to the dielectric quasi-TEM mode is that the element G_s in Fig. 4 dominates for most of the frequency components involved, and the line behaves like an LG line.

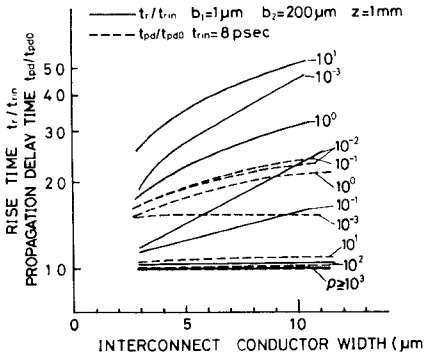

Fig. 8. Dependence of delay time and rise time on the interconnection strip width for a semi-infinite interconnection (or matched termination). The rise time of the input pulse is assumed to be 8 ps.

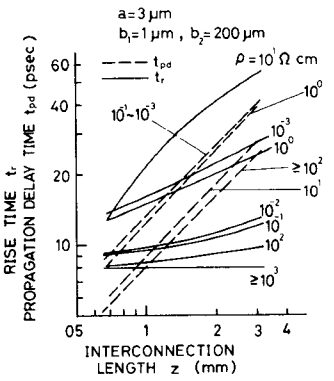

Fig. 9. Dependence of delay time and rise time on the distance z from the signal source on a semi-infinite interconnection (matched termination). The rise time of the input pulse is assumed to be 8 ps.

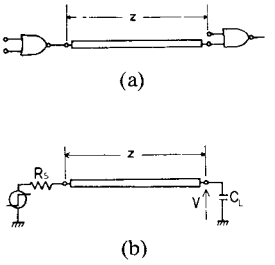

Fig. 10. (a) Interconnection between two logic gates and (b) its model. R_s is the effective signal source resistance of the first gate and C_L is the input capacitance of the second gate.

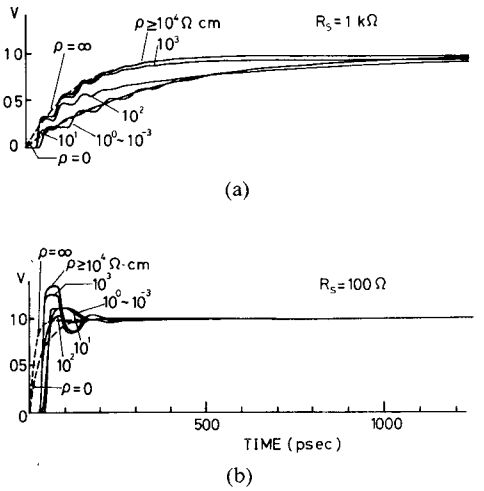

Fig. 11. Examples of step response waveform. (a) $R_s = 1$ kΩ and (b) $R_s = 100$ Ω. $a = 3$ μm, $z = 3$ mm, $b_2 = 1$ μm, $b_2 = 200$ μm.

Therefore, the wave propagation proceeds more or less like diffusion, resulting in a slow buildup of the pulse waveform.

The dependences of the delay time and rise time on the strip width are plotted in Fig. 8. Fig. 9 shows the dependences of the delay and rise time on the distance z. Rise-time deterioration near 10 Ω·cm is almost proportional to line length, and this reflects the above-mentioned diffusion-like nature of wave propagation.

C. Interconnections Between Logic Gates and Transient Waveforms

The present model was further applied to the situation where two logic gates are connected by an interconnection as shown in Fig. 10(a). For the calculation, the logic gate output was represented by its effective signal source resistance R_s, and the gate input was represented by an input capacitance C_L as shown in Fig. 10(b). It can be shown that, in the gates consisting of FET-type devices such as MOSFET's, MESFET's, and HEMT's, R_s is approximately equal to the inverse of the transconductance g_m of the switching or load transistor depending on which is taking part in the transient. As for the input capacitance, a standard 1-μm-gate GaAs MESFET has approximately a gate capacitance of 1 fF per 1-μm gatewidth.

Examples of the calculated transient waveforms of step response are shown in Fig. 11 (a) and (b). The 3-μm rule is assumed, and the interconnection length z is taken to be 3 mm. Dashed curves are the waveforms based on the "lumped capacitance" approximation for the interconnection, where two different capacitance values are used. One is based on the assumption that the semiconductor substrate can be regarded as the perfect insulator ($\rho = \infty$), and the other is on the assumption that it can be regarded as a perfect conductor ($\rho = 0$). It is seen that the "lumped capacitance" approximation is reasonably good, when the signal source impedance R_s is high and the response is slow. But, when R_s is low and a high-speed response is realized, the "lumped capacitance" approximation becomes excessively inadequate.

D. Effects of Substrate Resistivity and Device Transconductace

The calculated propagation delay time t_{pd} (delay up to 50-percent rise) and rise time (10–90-percent rise) as observed at the input of the second gate are summarized in Figs. 12 and 13, respectively. Those values, as obtained by the aforementioned two limiting cases of "lumped capacitance" approximation, are also shown by the dashed lines. It is more clearly seen in Figs. 12 and 13 that the "lumped capacitance" approximation is valid only in LSI/VLSI's with t_{pd} above 100–200 ps. In Fig. 12, the rise time is seen to become higher for large values of R_s and higher values of substrate resistivity than the upper dashed curve corre-

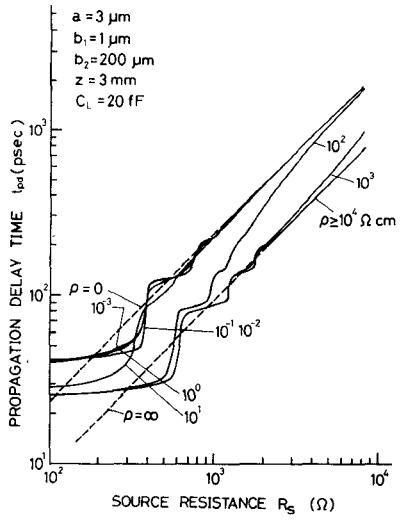

Fig. 12. Calculated delay time versus signal source impedance of gate R_s.

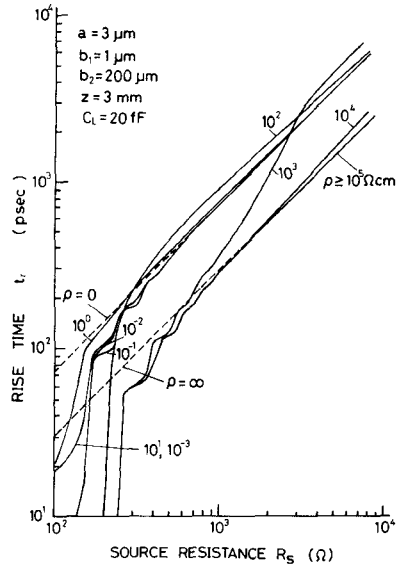

Fig. 13. Calculated rise time versus signal source impedance of gate R_s.

sponding to the "lumped capacitance" approximation with an insulator approximation for the substrate ($\rho = \infty$). This may appear physically unacceptable because the lumped capacitance approximation is expected to be valid in this region. However, it actually reflects the Maxwell–Wagner-type interfacial charge relaxation effect, and can be explained by including the "lumped conductance" of the substrate.

The results in Figs. 12 and 13 strongly indicate that semi-insulating substrates offer a significant advantage over semiconducting substrates in both delay and rise times. Particularly, rise-time deterioration due to mode transition from the slow-wave mode to the dielectric quasi-TEM mode, as explained previously, is very severe in the substrate resistivity range of 10^0–10^1 Ω·cm, requiring low source resistance R_s of 120–200 Ω to achieve t_r of below 100 ps. It should be noted that the above substrate resistivity range is actually employed in the current silicon technology. A factor of a 1.5–2 increase in delay is also caused by the slow-wave mode, if the resistivity is below 1 Ω·cm. Up to now, such effects have not been reported experimentally in Si IC's, but this is simply because the speed performance is still not fast enough to see them.

TABLE I
TRANSCONDUCTANCE g_m AND R_s OF VARIOUS FET DEVICES
(gate length = 1 μm; gate width = 10 μm)

DEVICE	g_m (mS)	R_S (Ω)
GaAs MESFET	1.4	710
Si MOSFET	0.8	1250
HEMT (77K)	2.9	350

Note: The data are converted from [24]. For comparison, a Si bipolar device with a 1×2-μm emitter size expected to have a g_m of 19.2 mS [24]. An AlGaAs/GaAs heterojunction bipolar transistor with a 4.5×10-μm emitter size exhibited a transconductance of 47.5 mS [25].

Another very important conclusion which can be drawn from Figs. 12 and 13 is that the strong driving capability of the device is essential in realizing very high-speed LSI/VLSI's. Table I summarizes typical values of the transconductance g_m and corresponding values of R_s for various switching devices (1-μm feature size) taken from the literature [24], [25]. It should be noted that in the conventional E/D or E/R gate configuration, R_s of the load devices should at least be 4–5 times of that of the switching device, and therefore the transient involving the load device limits the speed. It can be said that the driving capability of the currently available device is barely sufficient to realize LSI/VLSI's with t_{pd} of below 100 ps. HBT and HEMT technologies seem promising in this respect for future improvement. Since (1), for the interconnection length, more or less assumes a random logic configuration (such as gate arrays), an alternative approach to fully exploit the inherent speed advantage of the devices is to improve the chip architecture so as to avoid long interconnections.

IV. Conclusion

On-chip interconnection delay in very high-speed LSI/VLSI's is analyzed, using a MIS microstrip line model and its equivalent circuit representation which allows closed-form formulas in the frequency domain. The main conclusions of the present study are the following.

1) The lumped capacitance approximation of interconnections cannot be used in LSI/VLSI's with t_{pd} below 100–200 ps. Microwave considerations are required in the logic, circuit, and layout design of such very high-speed integrated circuits.

2) To drive interconnections at high speeds, the driving capability of the device per unit layout area is essentially important. Effective signal source resistance of the gate should be less than 500 Ω to achieve the propagation delay time of less than 100 ps in LSI/VLSI's on semi-insulating substrates where the average interconnection length is 1–3 mm.

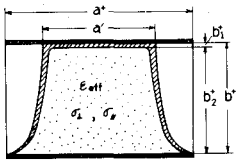

Fig. 14. The inhomogenous parallel waveguide mapped form the MIS microstrip line by Schwarz–Christoffel transformation.

3) The semi-insulating property of substrates offers a factor of 1.5–2 advantage in propagation delay time with a much steeper rise time for high-speed pulse transmission in LSI/VLSI's because of absence of the slow-wave mode and mode transition that are present in semiconducting substrates. To achieve the same speeds, semiconducting substrates require devices with larger driving capability.

Appendix
Determination of Equivalent Circuit Parameters

In the quasi-static limit, fields are determined by the Laplace equation. An unloaded single microstrip line with strip width a and height $b = b_1 + b_2$ can be tranformed to a parallel-plate waveguide by the following Schwarz–Christoffel (S–C) transformation:

$$W = -j\frac{\pi}{2K}W_1 - j\frac{2K'b}{\pi}Z\left(\frac{\pi W_2}{2b}\right)$$

$$h \equiv \left|\frac{dW}{dW_1}\right| = \left|E' - K'k^2\,\mathrm{sn}^2\,\frac{\pi W^2}{2b}\right| \qquad \text{(A1)}$$

where h is the scaling parameter of the transformation, Z is Jacobi's Zeta function, sn is Jacobi's elliptic function, and K' and E' are complete elliptic integrals of the first and second kinds with modulus k, respectively. Then, the present MIS microstrip line is mapped to the inhomogeneous parallel waveguide shown in Fig. 14 by the same S–C transformation. In terms of the length parameters in Fig. 14, the circuit elements are given by the following formulas:

$$C_1 = \frac{a^+}{b_1^+} = \epsilon_1\frac{a}{b_1} \qquad C_2 = \epsilon_{\mathrm{eff}}\frac{a^+}{b_2^+} \qquad G_s = \sigma_\perp\frac{a^+}{b_2^+}$$

$$L_1 = \mu_0\frac{b_1^+}{a'} \qquad L_2 = \mu_0\frac{b_2^+}{a^+ - a'} \qquad \text{(A2)}$$

where ϵ_{eff} and $\sigma_\perp$ are the effective dielectric constant and effective transverse conductivity reflecting partial filling, which are given in [14]. For the actual calculation of the length parameters, approximate formulas in [14] were used.

In order to include the skin effect more accurately in the evaluation of $Z_s(\omega)$, transformation of the Helmholtz equation for E_z is considered. The Helmholtz equation is generally variant under the S–C transformation. However, it can be regarded approximately invariant in the vicinity of the underneath of the strip, which is physically important for the skin effect under the following conditions. The conditions are that appropriate averaged values are assigned to the scaling parameter h of the S–C transformation and also to the effective longitudinal conductivity $\sigma_{\|}$ to be used in the transformed domain. This allows us to use the result of the parallel-plate waveguide analysis [14] in the transformed domain for the evaluation of the semiconductor impedance $Z_s(\omega)$. The resulting formulas are summarized as follows:

$$Z_s(\omega) = j\omega\mu_0\left(\frac{b_2^+}{a'}\right)\left(\frac{1}{\gamma_m b_2^+}\right)\tanh\gamma_m b_2^+$$

$$\gamma_m = \sqrt{j\omega\mu_0\sigma_{11}}$$

$$\sigma_{\|} = \sigma\bar{h}^2$$

$$\bar{h} = \sqrt{|E'(E' - K'k^2)|} \qquad \text{(A3)}$$

where $\bar{h}$ is the average scaling parameter between the center of the top plane and the center of the bottom plane in Fig. 14.

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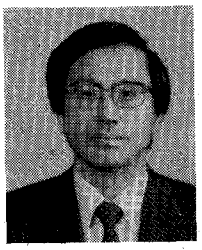

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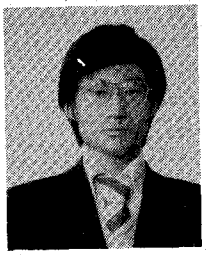

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